

## DECLARATION

I, NOBUAKI KATO, a Japanese Patent Attorney registered No. 8517, of Okabe International Patent Office at No. 602, Fuji Bldg., 2-3, Marunouchi 3-chome, Chiyoda-ku, Tokyo, Japan, hereby declare that I have a thorough knowledge of Japanese and English languages, and that the attached pages contain a correct translation into English of the priority documents of Japanese Patent Application No. 2004-099346 filed on March 30, 2004 in the name of CANON KABUSHIKI KAISHA.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 31<sup>st</sup> day of March, 2009



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NOBUAKI KATO

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Patent Office

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[Telephone Number] 03-3431-1831

[Indication of Official Fee]

[Prepayment Ledger No.] 010700

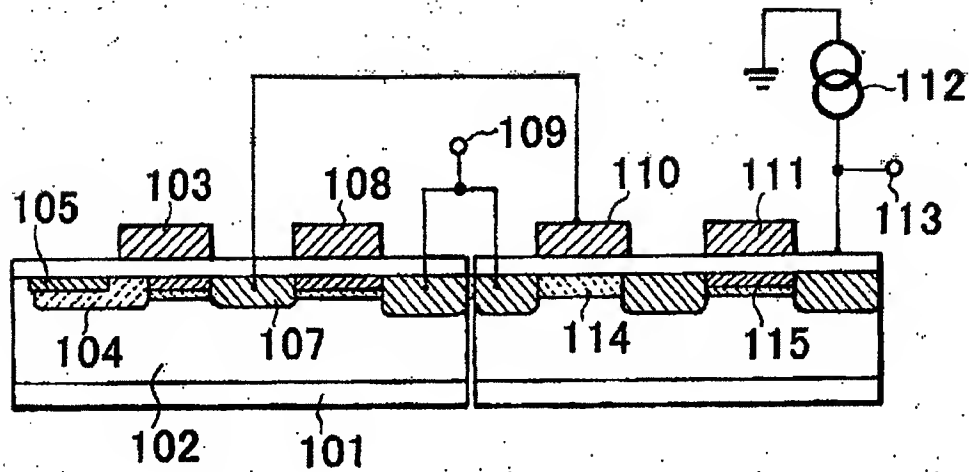
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[List of Filed Materials]

[Material]	Specification	1
[Material]	Drawings	1
[Material]	Abstract	1
[Material]	Claim	1
[Proxy Number]	0213163	

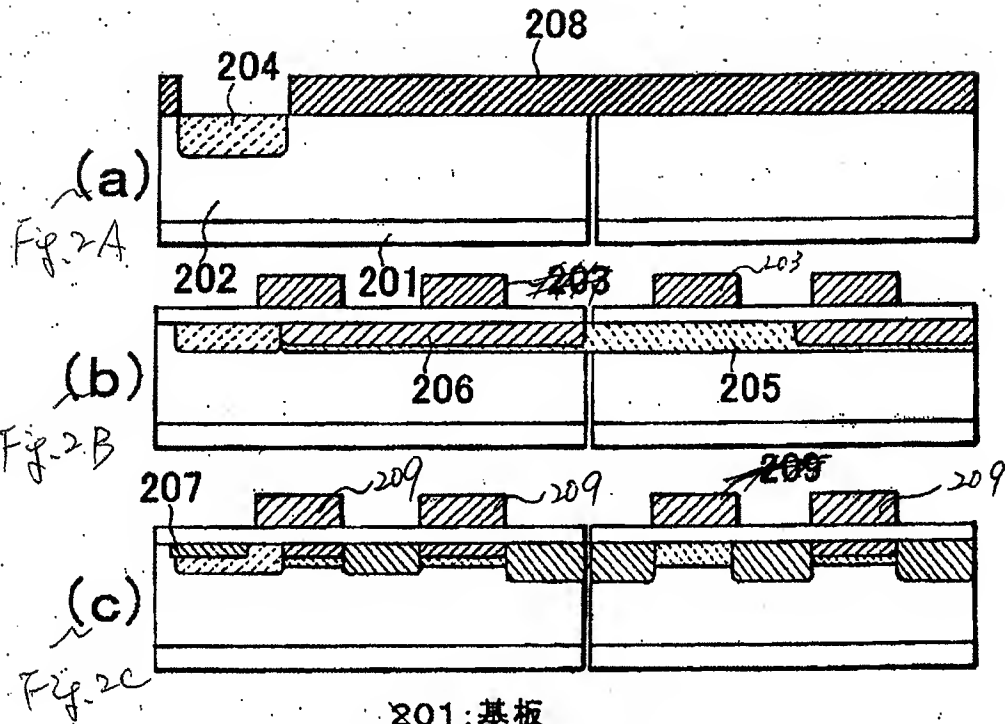
【書類名】 図面

【図1】



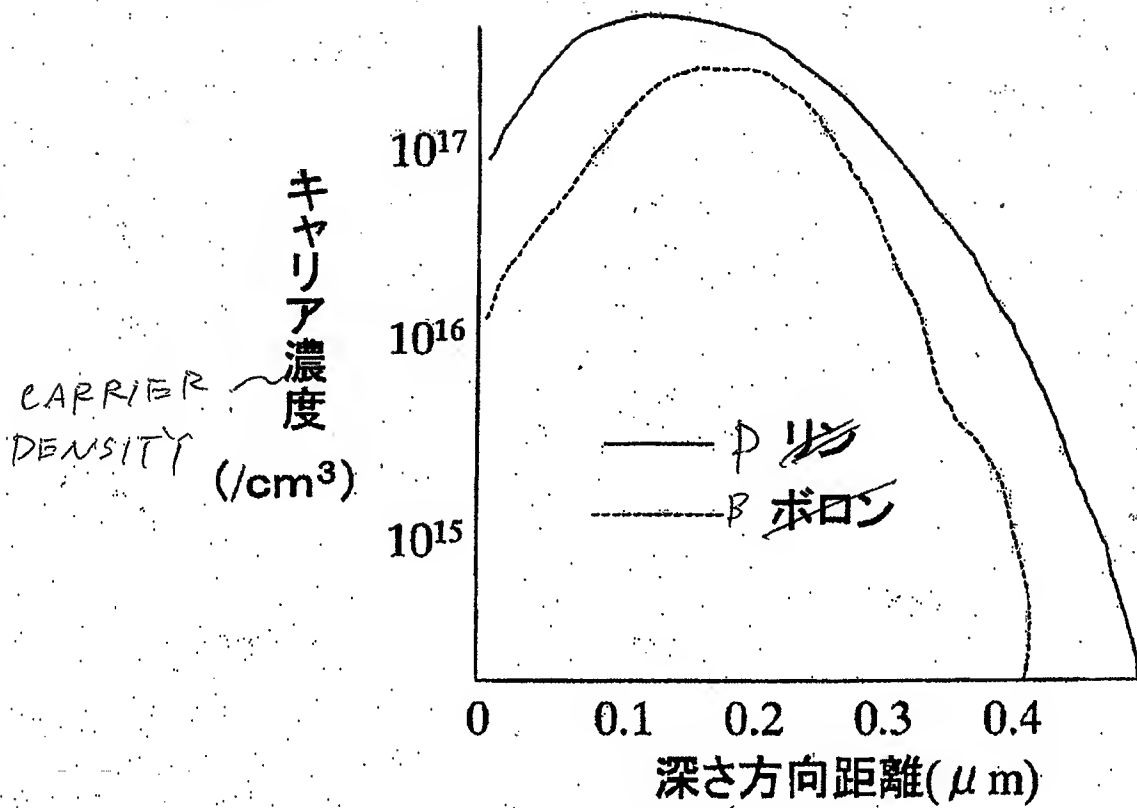
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- 102: ウエル
- 103: 制御電極
- 104: ホトダイオード部
- 107: 拡散浮遊領域
- 108: リセット用MOSトランジスタ
- 109: 電源
- 110: ソースフォロアトランジスタ
- 111: 行選択スイッチ用トランジスタ
- 112: 電流源
- 113: 出力端子
- 114: 第1のチャネルドーパント
- 115: 第2のチャネルドーパント

【図2】



- 201: 基板
- 202: ウエル
- 203: 制御電極
- 204: ホトダイオード部
- 205: 第1のチャネルドーパント
- 206: 第2のチャネルドーパント
- 207: 表面層
- 208: ホトレジスト
- 209: 制御電極

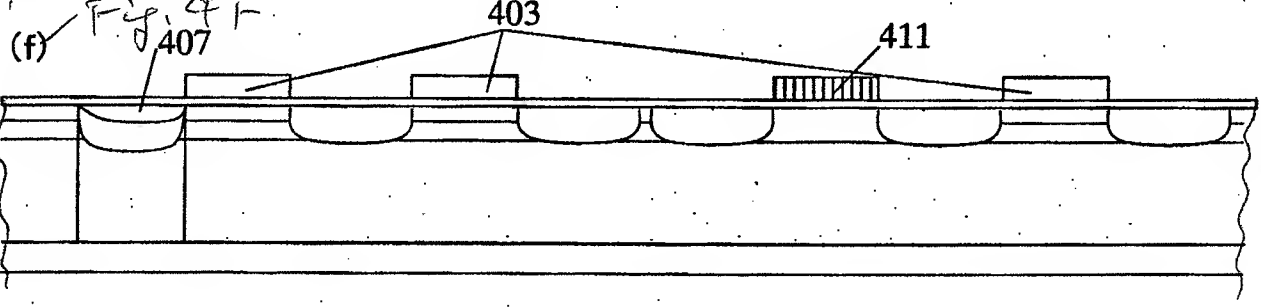
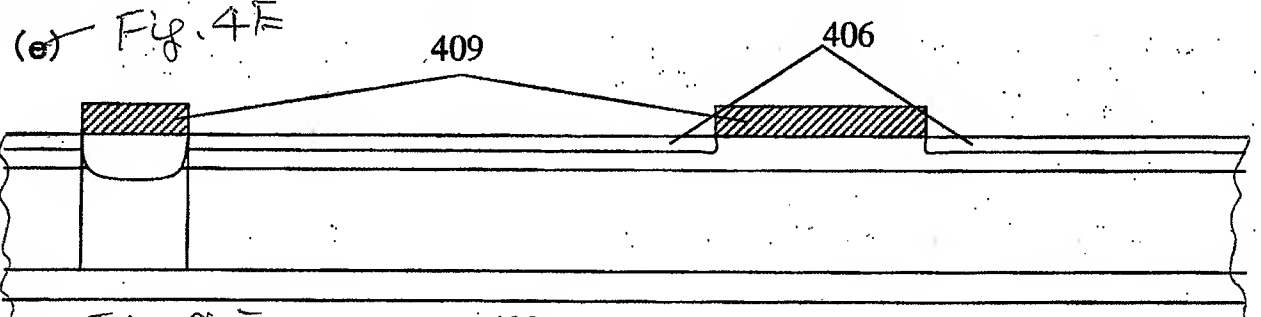
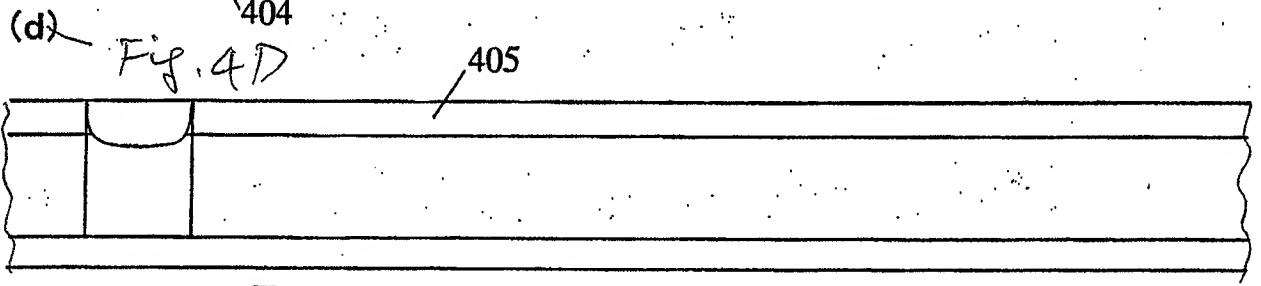
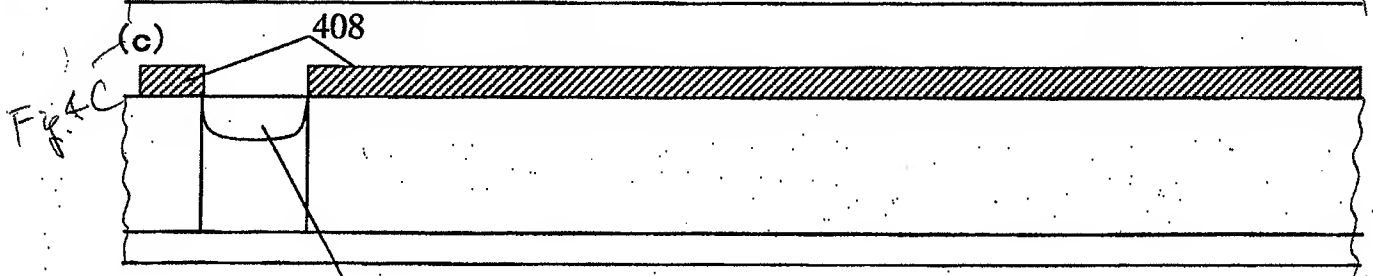
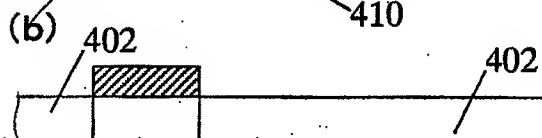
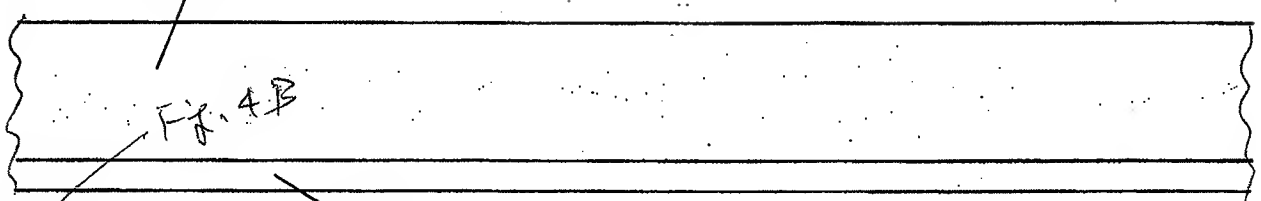
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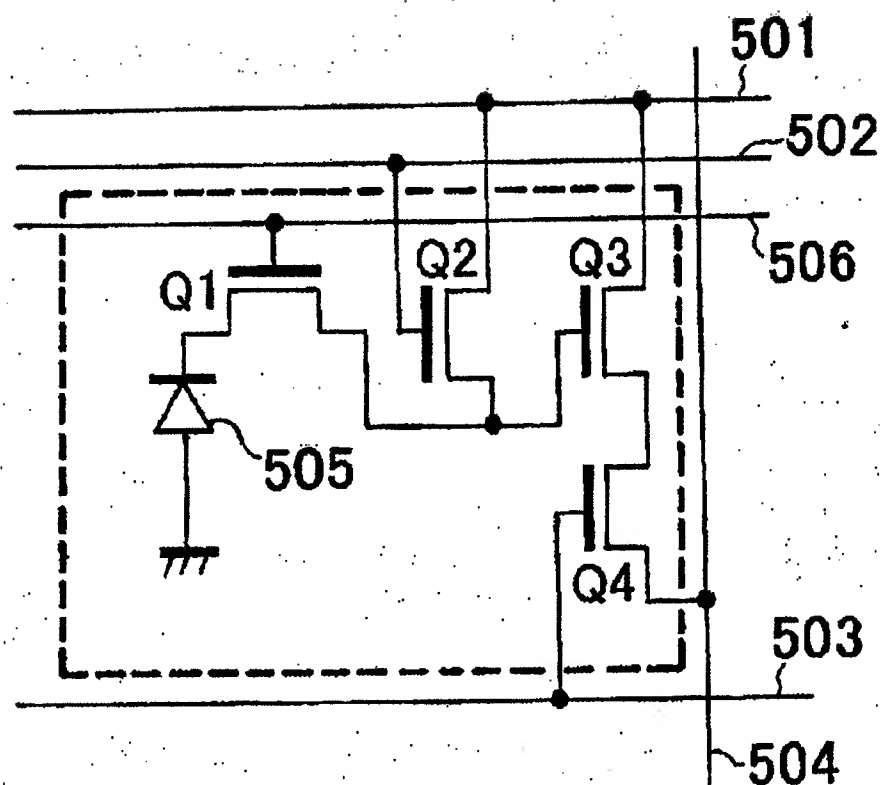
DISTANCE ( $\mu\text{m}$ ) IN ~~DEPTH~~  
DEPTH DIRECTION

(\*) 4

(a) Fig. 4A



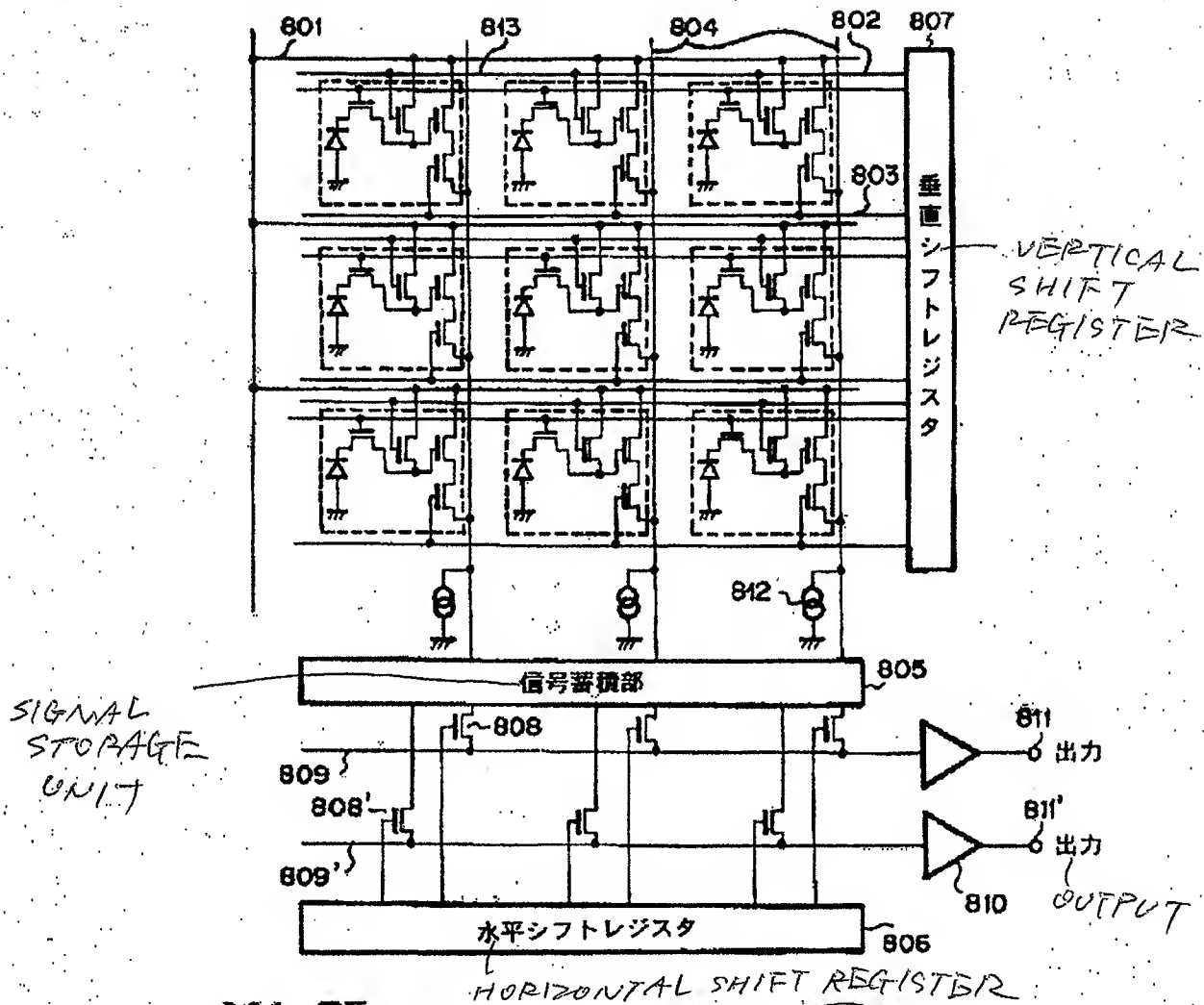
【図5】



- 501: 電源
- 502: リセットスイッチ線
- 503: 選択スイッチ線
- 504: 信号出力線
- 505: ホットダイオード
- 506: 転送スイッチ線

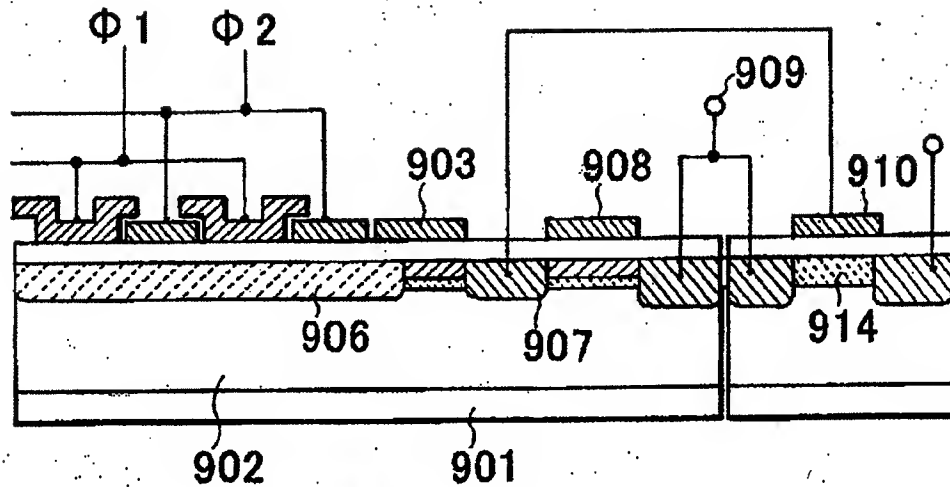


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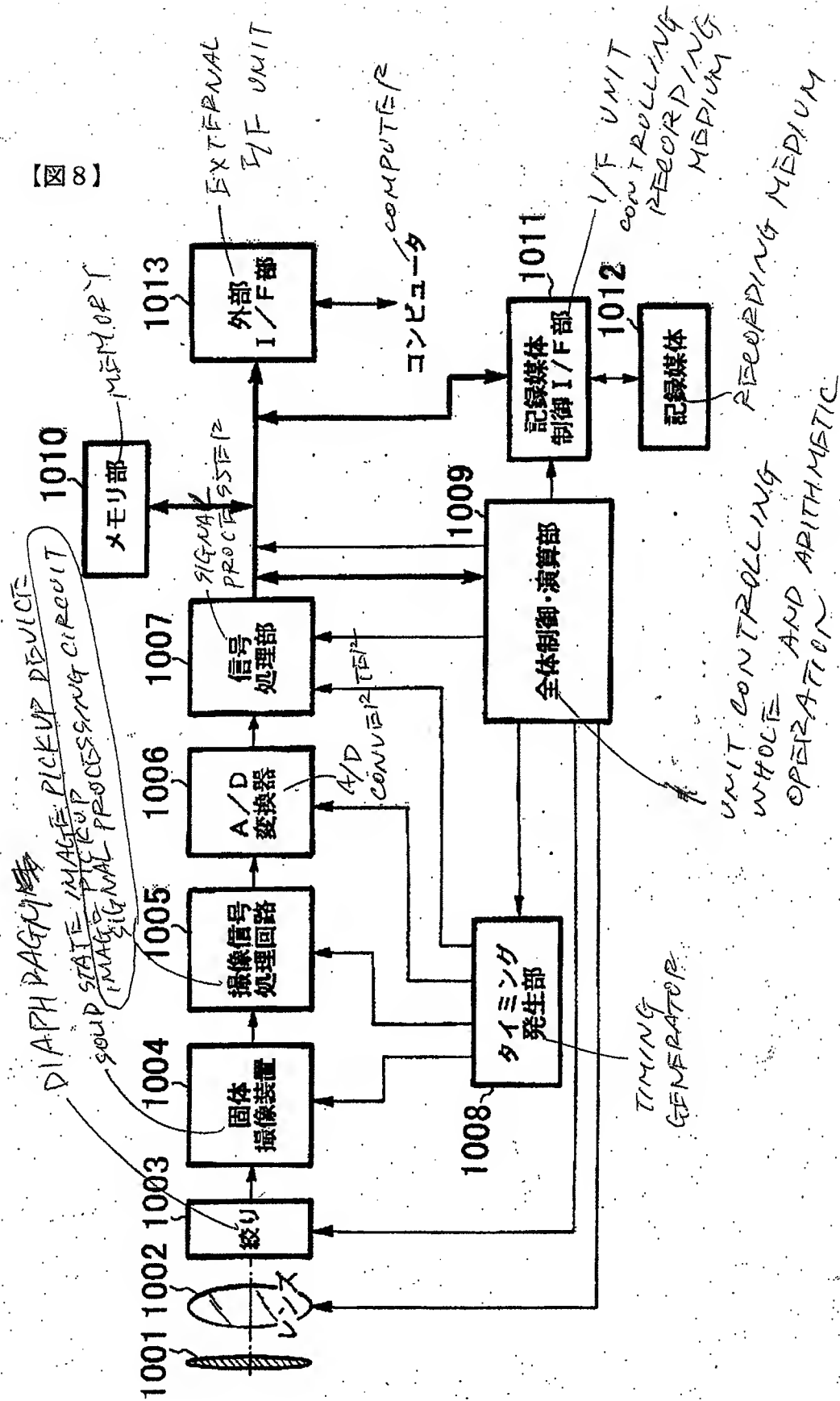
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| 802: リセットスイッチ線       | 809': 共通信号線2 |
| 803: 選択スイッチ線         | 810: 出力アンプ   |
| 804: 信号出力線           | 812: 定電流源    |
| 808: 共通信号線1への転送スイッチ  | 813: 転送スイッチ線 |
| 808': 共通信号線2への転送スイッチ |              |

【図7】

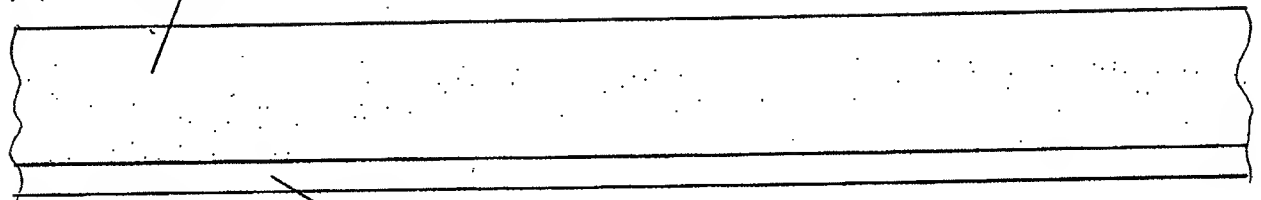


- 901: 基板
- 902: ウェル
- 903: 制御電極
- 906: 電荷転送部ウェル
- 907: 拡散浮遊領域
- 908: リセット用MOSTランジスタ
- 909: 電源
- 910: ソースフォロアトランジスタ
- 914: 第1のチャネルドープ

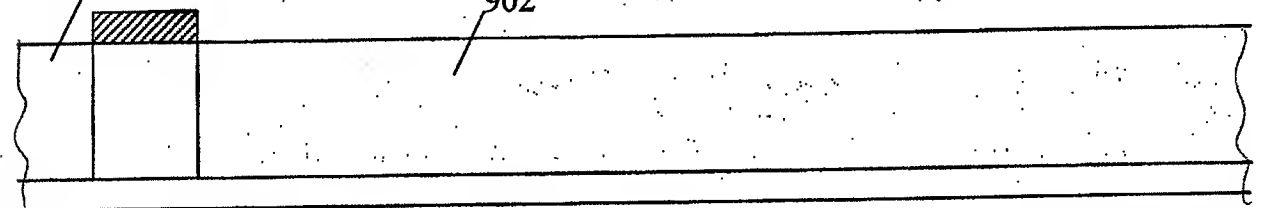
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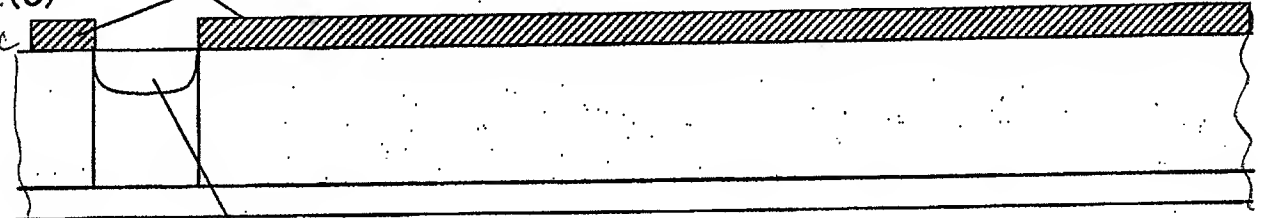
9  
(a) Fig. 9A 901



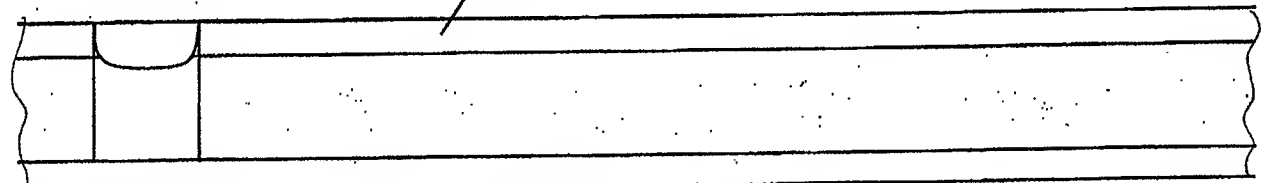
(b) Fig. 9B 902 910



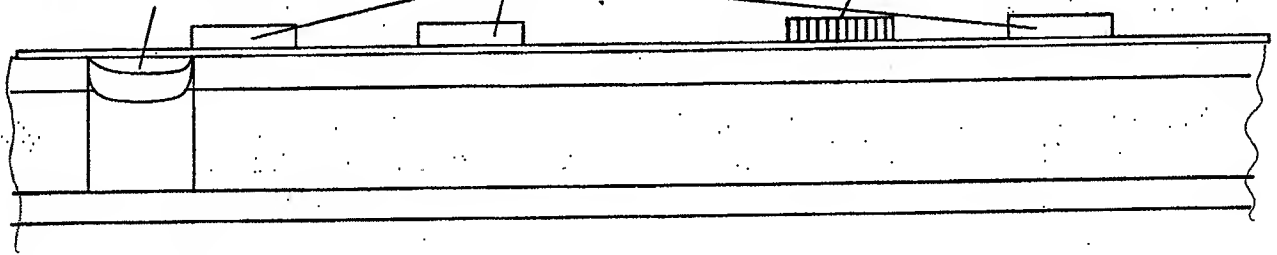
(c) Fig. 9C 908



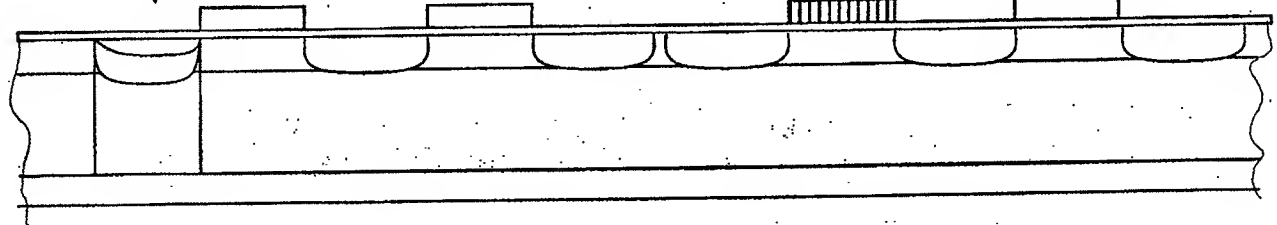
(d) Fig. 9D 905



(e) Fig. 9E 907 903 911



(f) Fig. 9F



2004-099346

[Name of the Document] What is claimed is:

[Claim 1]

5           A semiconductor apparatus provided with a  
buried channel type first conductive type MOS  
transistor and a surface channel type first  
conductive type MOS transistor formed on a substrate,  
wherein a first conductive type impurity region is  
10 provided in channel parts of said buried channel type  
and surface channel type MOS transistors.

[Claim 2]

          A solid state image pickup device comprising a  
pixel having a photoelectric conversion portion and a  
15 plurality of transistors formed in correspondence to  
said photoelectric conversion portion, on a substrate,  
wherein said plurality of transistors include a  
buried channel type first conductive type MOS  
transistor and a surface channel type first  
20 conductive type MOS transistor, and a first  
conductive type impurity region is provided in  
channel parts of said buried channel type and surface  
channel type MOS transistors.

[Claim 3]

25           A solid state image pickup device as claimed in  
claim 2, wherein said plurality of transistors  
include an amplifier transistor amplifying a signal

from said photoelectric conversion portion, and said amplifier transistor is constituted by said buried channel type MOS transistor.

[Claim 4]

5           A solid state image pickup device as claimed in claim 2 or 3, wherein said surface channel type MOS transistor has a second conductive type channel doped layer in the vicinity of its surface, in addition to a first conductive type channel doped layer.

10   [Claim 5]

          A solid state image pickup device as claimed in claim 4, wherein a doze amount of a first conductive type channel doped layer is smaller than a doze amount of a second conductive type channel doped layer.

15   [Claim 6]

          A solid state image pickup device as claimed in any one of claims 2 to 5, wherein the first conductive type is an n-type.

20   [Claim 7]

          A solid state image pickup device as claimed in claim 6, wherein a dopant of the first conductive channel doped layer is arsenic.

[Claim 8]

25           A solid state image pickup device as claimed in any one of claims 3 to 7, wherein the amplifier transistor is a source follower MOS transistor

present at an output stage of the pixel part.

[Claim 9]

A solid state image pickup device comprising a pixel part formed on a substrate and having a photoelectric conversion portion and an amplification MOS transistor formed corresponding to the photoelectric conversion portion to amplify a signal sent from the photoelectric conversion portion, wherein.

10 The amplification MOS transistor is a buried channel type transistor.

[Claim 10]

A method of manufacturing a semiconductor device comprising a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor, wherein

a first conductive type impurity region is formed in channel parts of the buried channel type MOS transistor and the surface channel type MOS transistor at the same step.

[Claim 11]

A method of manufacturing a solid state image pickup device comprising a pixel part formed on a substrate and having a photoelectric conversion portion and a plurality of transistors formed corresponding to the photoelectric conversion portion, wherein

the plurality of transistors include a buried channel type first conductive MOS transistor and a surface channel type first conductive MOS transistor and a first conductive type impurity region is formed  
5 in channel parts of the buried channel type first conductive MOS transistor and the surface channel type first conductive MOS transistor at the same step.  
[Claim 12]

A solid state image pickup device manufacturing  
10 method as claimed in claim 11, wherein a second conductive type impurity region is formed in the channel part of the surface channel type MOS transistor.  
[Claim 13]

15 A solid state image pickup device manufacturing method as claimed in claim 12, wherein the dose amount of a first conductive type channel doped layer is smaller than that of a second conductive type channel doped layer.

20 [Claim 14]

A solid state image pickup device manufacturing method as claimed in any one of claims 11 to 13, wherein the first conductive type is an n-type.  
[Claim 15]

25 A solid state image pickup device manufacturing method as claimed in claim 14, wherein a dopant of the first conductive channel doped layer is arsenic.



[Claim 16]

An image pickup system comprising:

an image forming optical system forming an  
image from a light from an object;

5       the solid state image pickup device as claimed  
in any one of claims 2 to 9 for converting the formed  
image in a photoelectrical manner; and

a signal processing circuit for digitally  
converting an output signal from the solid state  
10 image pickup device.

[Name of the Document] Specification

[Title of the Invention] Semiconductor Device, Solid  
State Image Pickup Device Using the Same and Method  
of Manufacturing them

5

[Technical Field]

[0001]

The present invention relates to a  
semiconductor apparatus and a solid state image  
10 pickup device using the same, and more particularly  
to a CMOS image sensor and a method of manufacturing  
the same.

[Background Art]

15 [0002]

As a typical solid state image pickup device,  
there are apparatuses called as a CCD sensor  
constituted by a photodiode and a CCD shift register,  
and a CMOS sensor such as an active pixel sensor  
20 (APS) constituted by a photodiode and a MOS  
transistor, and the like.

[0003]

The APS includes a photodiode, a MOS switch, an  
amplifier circuit for amplifying a signal from the  
25 photodiode and the like in each pixel. Further, the  
APS has a lot of advantages such that an XY  
addressing can be executed and a sensor and a signal

processing circuit can be formed as one chip.

However, on the other hand, since a number of devices within one pixel is large, a pixel aperture ratio is small. Further, it is hard to reduce a chip size  
5 which determines a magnitude of an optical system, and the CCD accounts for a large percentage of a market.

[0004]

In recent years, the CMOS sensor draws the  
10 attention on the basis of an improvement of a micro forming technique of the MOS transistor and an increase of requests for making the sensor and the signal processing circuit by one chip and making an electric power consumption low.

15 [0005]

Fig. 5 shows an example of an equivalent circuit of the APS (for example, see Patent Literature 1). The structure of the prior art will be briefly described.

20 [0006]

Reference numeral 501 denotes a power source line, reference numeral 502 denotes a reset switch line selecting a reset transistor, reference numeral 503 denotes a select switch line selecting a select  
25 transistor, reference numeral 504 denotes a signal output line, reference numeral 505 denotes a photodiode serving as a photoelectric conversion

portion, reference numeral 506 denotes a transfer switch line for selecting a transfer transistor, reference symbol Q1 denotes a transfer transistor, reference symbol Q2 denotes a reset transistor, reference symbol Q3 denotes a transistor for selection, and reference symbol Q4 denotes a select transistor. The photoelectric conversion portion corresponds to an embedded type photodiode used in a CMOS, CCD or the like. The embedded type photodiode is structured such that a region having a high impurity density (for example, a p-type layer) is provided in a surface. Accordingly, it is possible to restrict a dark current generated in an SiO<sub>2</sub> surface, a junction capacitance can be provided between a storage unit (for example, an n-type layer) and the p-type layer in the surface, and it is possible to increase a saturation charge amount of the photodiode.

[0007]

A light signal charge  $Q_{sig}$  stored in the photoelectric conversion portion 505 is read in a floating diffusion area via a transfer unit Q1 constituted by a MOS transistor. The element Q2 resets an electric potential of the floating diffusion area.

[0008]

The charge is voltage converted into a signal

charge  $Q_{sig}/CFD$  on the basis of a capacity  $CFD$  of the floating diffusion area, and the signal is read through the source follower circuit  $Q3$ .  $Q4$  is a select switch for selecting a line.

5 [0009]

There has been proposed a solid state image pickup device using the buried channel type MOS transistor as the reset transistor and the transfer transistor (for example, see Patent Literature 2).

10 [Patent Literature 1] Japanese Patent Application Laid-Open No. 11-274454

[Patent Literature 2] Japanese Patent Application Laid-Open No. 2001-309243  
[Disclosure of the Patent]

15 [Problems to be Solved by the Invention]  
[0010]

However, the prior art has such a problem that a noise component is included in an output voltage due to a  $1/f$  noise generated in the transistor  $Q3$  in a source follower portion. Accordingly, there has been proposed a method of forming the source follower portion in the final stage by a buried channel type pMOS transistor

25 However, a process becomes complicated and a cost increase is caused.

Further, not being limited to the solid state image pickup device, in the case that the surface

channel type MOS transistor and the buried channel type MOS transistor are both provided within the chip, there has been a problem that a manufacturing process thereof becomes complicated.

5 [0011]

Accordingly, an object of the present invention is to provide a semiconductor device which is reduced in noise by forming a highly controllable transistor by a simple process and its manufacturing method.

10 [Means for Solving the Problems]

[0012]

In order to achieve the object mentioned above, in accordance with the present invention, there is provided a semiconductor apparatus having both a  
15 buried channel type first conductive MOS transistor and a surface channel type first conductive MOS transistor, wherein a first conductive type channel doped layer exists near a surface in both of the buried channel type and surface channel type MOS  
20 transistors. As a result, a transistor whose  $1/f$  noise is to be reduced can be formed in a needed position. This effect is exhibited noticeably in a noise-sensitive solid state image pickup device. Further, in the case of using the buried channel type  
25 transistor in a source follower type MOS transistor in an output portion of a solid state image pickup device, it is possible to form a solid state image

pickup device having a reduced noise, and this structure is particularly effective in the case that the source follower MOS transistor is provided in the pixel portion as in a CMOS image sensor. The surface  
5 channel type transistor preferably has a second conductive type channel doped layer in the vicinity of its surface, in addition to a first conductive type channel doped layer, by which simultaneous formation of transistors which are excellent in off-  
10 characteristic is realized. The dose amount of the first conductive type channel doped layer is preferably smaller than that of the second conductive type channel doped layer.

[0013]

15 In addition, the first conductive type is an n-type and the first conductive type channel doped layer is preferably made of arsenic. As a result, there can be formed a highly controllable semiconductor device.

20 [0014]

Further, since both the buried channel type first conductive MOS transistor and the surface channel type first conductive MOS transistor are provided and the first conductive type channel doped  
25 layer is formed by implanting ions into both the buried channel type and surface channel type MOS transistors in the vicinity of their surfaces at a

single step, highly controllable transistors can be formed by a simple process. As a result, there can be provided a semiconductor device reduced in cost and noise.

5 [Effect of the Invention]

[0015]

According to the present invention, since both the buried channel type first conductive MOS transistor and the surface channel type first  
10 conductive MOS transistor are provided and the first conductive type channel doped layer is present in both the buried channel type and surface channel type MOS transistors in the vicinity of their surfaces, a transistor whose  $1/f$  noise is to be reduced can be  
15 formed in a needed position and hence there can be formed a semiconductor device which is reduced in noise. Preferably, the surface channel type transistor has a second conductive type channel doped layer in the vicinity of the surface in addition to  
20 the first conductive type channel doped layer, by which simultaneous formation of transistors which are excellent in off-characteristic becomes possible.

[0016]

Since the buried channel type first conductive  
25 MOS transistor and the surface channel type first conductive MOS transistor are provided and the first conductive type channel doped layer is formed both



in the buried channel type and surface channel type MOS transistors in the vicinity of their surfaces by ion implantation, a highly controllable transistor can be formed at one step and hence there can be  
5 provided a semiconductor device which is reduced in cost and noise.

[Best Mode for Carrying Out the Invention]

[0017]

10           Next, a description will be given of a best mode of the present invention with reference to the accompanying drawings, by exemplifying a solid state image pickup device.

[0018]

15           Fig. 1 is a view of a cross sectional structure best showing features of the present invention. In Fig. 1, a photoelectric conversion device is constructed such that a p-type well 102 is formed on an n-type substrate 101, a thin n-type layer is  
20 formed on the well 102, an n-type layer 104 of a photodiode is formed on the layer, an n-type layer 105 serving as a buried region is formed on the layer 104 and a gate region 103 of a transfer MOS transistor is formed on a side face of the photodiode  
25 via an insulating layer.

[0019]

A diffusion floating region FD 107 is formed

under the side face of the transfer MOS transistor gate region 103 and is connected to a gate of a MOS transistor for amplification of an output circuit, a drain of a MOS transistor 111 for line selection switch is connected to a source of the amplification MOS transistor, a current source 112 as a load of the amplification MOS transistor is connected to a source of the line selection switch MOS transistor 111 to constitute a source follower amplifier circuit. As the transistor 110 of the source follower amplifier circuit, a buried channel type MOS transistor is used to reduce  $1/f$  noise. Here, the buried channel type MOS transistor is a MOS transistor in which an impurity region of the same conductive type as a source and drain region is formed also in a channel region directly under the gate.

[0020]

A source of a reset MOS transistor 108 for resetting the diffusion floating region FD 107 is connected to the diffusion floating region FD 107 and a reset power source 109 is connected to a drain of the transistor 108. The other MOS transistors than the source follower transistor are constituted here, for example, by a surface channel type MOS transistor having a threshold voltage of 0.4 V.

[0021]

Next, a description will be given in detail of

the feature of the present invention while describing a reading operation. An electron which is generated by an incident light in accordance with a photoelectric conversion is stored in the n-type layer. At this time, the transfer MOS transistor is in an OFF state. After a predetermined storing time has passed, a positive voltage is applied to the control electrode (gate electrode) 103 of the transfer MOS transistor so as to set the transfer MOS transistor in an ON state, and a stored charge in the n-type layer 107 of the photodiode is transferred to the diffusion floating region 107. Before setting the transfer MOS transistor to the ON state, the diffusion floating region is reset to a predetermined voltage. When the stored charge is transferred to the diffusion floating region, the voltage of the diffusion floating region is lowered at a degree of  $Q_{sig}/CFD$  from the reset voltage in the case of using a transfer charge  $Q_{sig}$  and a diffusion floating region capacity  $CFD$ , because the transfer charge is constituted by the electron. If the storing layer of the photodiode is of the p-type, the transfer charge is constituted by a hole and the voltage is inversely increased.

[0022]

In the APS mentioned above, it is possible to remove most of the noise component in the reset noise

of the diffusion floating region 107 by temporarily holding an output signal  $V_{r1}$  generated directly after resetting the diffusion floating region 107 and taking a difference between the signal  $V_{r1}$  and an  
5 output signal  $V_{sig1}$  obtained by superposing the component  $Q_{sig}/CFD$  on the reset signal or by using a buried channel type MOS transistor as the source follower MOS transistor. In particular, in the case that the photodiode and the transfer MOS transistor  
10 103 satisfy a condition mentioned below, it is possible to achieve a higher noise rejection ratio. In other words, it is important to read the signal charge stored in the n-type layer at a higher rate.  
[0023]

15 A description will be given in detail. A voltage of the diffusion floating region which is lowered at a voltage of  $Q_{sig}/CFD$  from the reset voltage after reading the signal is set to  $V_{FDsig1}$ . In this case, if the transfer MOS transistor is in a  
20 sufficient ON state, a reverse bias of the  $V_{FDsig1}$  is applied to a GND potential in the p-type well and the p-type layer having the high surface impurity density, in the n-type layer of the photodiode. At this time, a depletion layer extends to the n-type layer from  
25 the p-type well and the p-type layer having the high surface impurity density, and an entire of the n-type layer of the photodiode is depleted, whereby it is

possible to read the signal charge in the diffusion floating region with hardly remaining the signal charge in the photodiode.

In this case, at the same time of reading the  
 5 signal charge in the diffusion floating region, the reset of the photodiode is executed. After reading, that is, in a state in which the reverse bias of the VFDsig1 is applied to the n-type layer of the photodiode, it is assumed that a number of the  
 10 electron remaining in the n-type layer is 0. Accordingly, it is possible to completely remove the reset noise by acquiring the difference between the output signal Vr1 just after the reset and the output signal Vsig1 obtained by superposing the component  
 15 Qsig/CFD on the reset signal. Further, it is possible to obtain an output signal obtained by an expression  $V_{sig1} - V_{r1} = Q_{sig}/CFD \times A$  (reference symbol A denotes a gain of an output circuit existing in each of the pixels).

20 [0024]

A noise  $\Delta V_{n1}$  of the output circuit existing in each of the pixels such as a 1/f noise or the like is superposed on the output signal. Further, a noise  $\Delta V_{n2}$  in a reading system after the output circuit in  
 25 each of the pixels is superposed on the output from an integrated circuit IC formed as a final area sensor.

[0025]

In order to achieve the reading mentioned above, it is necessary to apply the reverse bias to the n-type semiconductor region of the photodiode and set a relation  $V_{dep} < V_{sign1}$  in which the voltage making the entire of the n-type layer to deplete is set to  $V_{dep}$ . In this case, the depletion voltage of the photodiode broadly means a reverse bias voltage satisfying a relation stored charge number in storage unit  $<$  net impurity number. Ideally, a number of the electrons remaining in the n-type layer of the photodiode after reading is 0, however, it is a design matter how much the reading is executed.

The  $\Delta V_{n1}$  is subject to the  $1/f$  noise or the like. In this case, there can be considered a method of making a gate oxide film thin, a method of clarifying the surface and the like.

However, if the buried channel type MOS transistor is employed, a very great effect can be obtained. Substantially, if the noise  $\Delta V_{n1}$  in the photodiode part is sufficiently smaller than the noise  $\Delta V_{n2}$  in the reading system, the noise component will be subject to the noise  $\Delta V_{n2}$ .

[0026]

In the case of forming the buried channel type MOS transistor constituting the transistor of the source follower part, an impurity 114 of the same

conductive type as the source drain region is doped in the channel portion, and a lowest potential region is formed in a region which is slightly deeper than the surface. In order to keep a low cost, it is  
5 necessary to execute a channel doping step of the buried channel type transistor without executing a patterning.

In order to minimize an effect applying to the other transistors, it is necessary to reduce a doping  
10 amount. In order to reduce the doping amount, it is preferable to employ the well of the same conductive type as the source drain region as the well. In this case, the structure tends to be made such that the transistor does not turn off even at the gate voltage  
15 of 0 V, however, there is no problem in view of the way of using the source follower. It is preferable to use in a range in which a linearity is kept.

There is a case that an off characteristic and a low substrate bias effect are required in the other  
20 transistors than the source follower portion.

In the off characteristic, a threshold voltage is controlled by doping a conductive type impurity  
115 which is different from the impurity 114 in the channel part. In comparison with the same conductive  
25 type channel doping amount as the impurity 114 used in the buried channel type MOS transistor, the different conductive type impurity 115 is injected

more to the normal surface channel type transistor. Accordingly, it is possible to increase the threshold voltage so as to be an enhance type. In view of a depth, the doped region for the buried channel is  
5 formed slightly deeper from the surface, and the doped region for the surface channel is formed in a region closer to the surface. In accordance with this structure, it is possible to realize the same conductive type channel doping as the impurity region  
10 for the buried channel in one step without patterning. As a result, the process can be simplified and hence cost reduction can be realized. In addition such effects can be also obtained that the density of impurity in the substrate under the channel part can  
15 be reduced and hence substrate biasing effect can be also reduced.

[0027]

In this case, the first conductive type is not particularly limited. It is preferably of the n-type,  
20 and a dopant to the buried channel is preferably constituted by an arsenic in view of a controllability since a sharp profile to a shallow portion can be obtained. Further, it goes without saying that the conductive type of the well is not  
25 particularly limited, and it may be constituted by the different conductive type well. A description will be given in detail of embodiments.



## Embodiment 1

[0028]

A description will be given of an embodiment 1 with reference to (a) to (c) of Fig. 2. A photodiode and a periphery thereof in accordance with the present embodiment are formed in accordance with the following procedure.

[0029]

An n-type well 202 having a surface density of  $2 \times 10^{16} \text{ cm}^{-3}$  is formed by implanting boron to a p-type substrate 201 by using an ion implanter, and applying a heat treatment. Next, a p-type layer 204 of the photodiode is formed by forming a photo resist 208 ((a) of Fig. 2).

[0030]

A p-type first channel doped region 205 is formed in an entire surface of the substrate by forming a gate oxide film in an entire surface of the substrate surface and thereafter implanting a boron at a doze amount of  $2\text{E}12 \text{ cm}^{-2}$  and 35 keV in accordance with an ion implanting method. Next, an n-type second channel doped region 206 is formed by forming a photo resist in a region forming the buried channel type MOS transistor, and implanting a phosphor at  $6\text{E}12 \text{ cm}^{-2}$  and 50 keV. An impurity profile of the buried channel portion and the surface channel portion is shown in Fig. 3.

In the buried channel portion, a potential is determined on the basis of the gate voltage and the density profile of the boron, and a valley of the potential exists at a position apart from the surface so as to achieve the buried channel. On the other hand, the phosphor is dominant as the impurity in the surface channel type so as to determine the channel, however, a carrier is cancelled by the boron in the lower portion of the channel, and a carrier density becomes small to reduce the substrate bias effect.

[0031]

Next, a control electrode 203 of the source follower MOS transistor or the transfer MOS transistor is formed by peeling the photo resist, thereafter forming a poly-silicon control electrode in which the phosphor is doped, and executing the patterning ((b) of Fig. 2). Next, the photo resist is formed on the photodiode of the substrate surface and on the other region of a part of the control electrode, and an n-type layer 207 having a high impurity density is formed in the surface by using the control electrode 203 as a mask.

[0032]

Next, the source train region is formed by ion implanting the boron to the p-type MOS transistor. Thereafter, the surface channel type MOS transistor is formed by covering the buried channel type MOS

transistor by the photo resist, thereafter ion implanting the boron further, and making the polysilicon control electrodes in a p-type (209).

[0033]

5           In this step, the source drain region of the normal p-type MOS transistor including the peripheral circuit portion (not shown) is formed. The n-type MOS transistor is formed in accordance with the normal semiconductor process ((c) of Fig. 2).

10   [0034]

          Thereafter, there are formed sequentially a first interlayer isolation film, a contact, a first metal wire, a second interlayer isolation film, a via connecting the first metal wire and the second metal  
15   wire, a second metal wire and a passivation film in accordance with the normal semiconductor manufacturing step.

[0035]

          As a result, it became possible to  
20   independently set the threshold voltages of the buried channel type pMOS transistor in which the polycrystalline silicon control electrode is constituted by an n-type diffusion electrode and the surface type MOS transistor in which the  
25   polycrystalline silicon control electrode is constituted by a p-type diffusion electrode. The noise can be lowered to about one third in the case

that the buried channel type MOS transistor is used in the source follower portion as in the present embodiment in comparison with the noise in the source follower portion in the case that all are formed by the surface channel type MOS transistor, whereby an improve characteristic can be obtained. Further, since the impurity density below the channel portion is also low in the surface channel MOS transistor, it became possible to obtain an improved output characteristic having a small substrate bias effect.

#### Embodiment 2

[0036]

A description will be given of an embodiment 2 with reference to Fig. 4. A photodiode and a periphery thereof in accordance with the present embodiment are formed in accordance with the following procedure.

[0037]

A deep p-type well 410 is formed by implanting a boron by using an ion implanter to an n-type substrate 401. Next, a potential blocking layer to the n-type and a well 402 of the surface channel type MOS transistor is prepared by ion implanting the boron to the other portions than the photo diode portion after the resist patterning. Next, a photo resist 408 is formed, and an n-type layer 404 of the photo diode is formed ((a) of Fig. 4).

[0038]

A first channel doped region 405 is formed by implanting arsenic to an entire surface of the substrate at a dose amount of  $6 \times 10^{11} \text{ cm}^{-2}$  and 60 keV without executing the patterning in accordance with an ion implanting method. Further, a second channel doped region 406 is formed by forming a photo resist in the buried channel portion and ion implanting boron to a channel portion for the surface channel at  $2 \times 10^{12} \text{ cm}^{-2}$  and 20 keV. In the buried channel type, the potential is determined on the basis of the density profile, the gate voltage and the voltage of the p-type well 402, and a valley of the potential exists at a position apart from the oxide film surface, and the buried channel is achieved as a path of the carrier. On the other hand, the boron is dominant as the impurity in the surface channel type and determines the potential. This is because the density of the boron is made larger in comparison with the density of the arsenic.

[0039]

After forming the gate oxide film in an entire surface of the substrate surface, the patterning is executed by forming the poly-silicon control electrode 402 in which the phosphor is doped at a high density ((b) of Fig. 4). Next, a p-type layer 407 in which a surface impurity density is high is

formed by forming a drain pattern of the photo resist on the photodiode of the substrate surface and in a partial region of the control electrode, by using the control electrode 403 as the mask.

5 [0040]

Thereafter, there are formed an n-type MOS transistor and a p-type MOS transistor, including the peripheral circuit portion (not shown) in accordance with the normal semiconductor process ((c) of Fig. 4).

10 [0041]

Further, there are formed sequentially a first interlayer isolation film, a contact, a first metal wire, a second interlayer isolation film, a via connecting the first metal wire and the second metal wire, a second metal wire and a passivation film in accordance with the normal semiconductor manufacturing step.

[0042]

As a result, it is possible to independently control and form the threshold voltages of the buried channel type pMOS transistor formed in the source follower portion and the other surface channel type MOS transistors. The noise can be lowered to about one third in the case that the buried channel type MOS transistor is used in the source follower portion as in the present embodiment in comparison with the noise in the source follower portion in the case that

20  
25

all are formed by the surface channel type MOS transistor, whereby an improve characteristic can be obtained. As is different from the embodiment 1, since the n-type MOS transistor is used in the pixel  
5 portion, a working speed is high, and the carrier generated by the light in the photo diode is constituted by the electron. Since a vessel having a larger potential is formed, a sensitivity is widely improved.

10 Embodiment 3

[0043]

There is manufactured an area sensor which uses a photodiode 505 and a transfer MOS transistor Q1 in accordance with the embodiments 1 and 2, is  
15 constituted by a pixel structure shown in Fig. 5 and is constituted by a read circuit shown in Fig. 6.

[0044]

In Fig. 5, the photodiode 505 and a transfer switch Q1 of the transfer MOS transistor transfer are  
20 provided. Reference symbol Q2 denotes a reset switch of a reset MOS transistor for resetting a diffusion floating region, reference symbol Q3 denotes an input MOS transistor of a source follower amplifier circuit formed by a buried channel type MOS transistor  
25 connected to the gate in the diffusion floating region and connected as a load of a source side, and reference symbol Q4 denotes a selecting switch for

selecting a read pixel.

[0045]

Fig. 6 shows a solid state image pickup device in which the pixel cell of the photoelectric conversion device structured by them is used in three rows and three lines.

[0046]

A description will be given below of a basic operation of Figs. 5 and 6. There are executed a reset operation of inputting a reset voltage to an input gate of the source follower by the reset switch Q2, and a row selection by the selecting switch Q4.

[0047]

A gate in a floating diffusion region of an input node of the source follower is set to a floating, a noise component constituted by the reset noise and a fixed pattern noise such as a dispersion of the threshold voltage of the source follower MOS and the like are read, and an information thereof is temporarily stored in a signal storage unit 805.

[0048]

Thereafter, the transfer switch Q1 is opened and closed, a stored charge of the photodiode generated by the light signal is transferred to the input node of the source follower, and a sum of the noise component mentioned above and the light signal component is read, and is stored in the signal



storage unit 805.

[0049]

A signal of the noise component and a signal of the sum of the noise component and the light signal component are respectively read to common signal lines 809 and 809' via transfer switches 808 and 808' to the common signal line by conducting the transfer switch of a common signal line 1 (808) and a common signal line 2 (808'), and are respectively output as outputs 811 and 811' via each of output amplifiers 810.

[0050]

Thereafter, the light signal component is taken out by removing the reset noise and the fixed pattern noise by acquiring a difference between the outputs 811 and 811', and it is possible to obtain an image pickup signal having a high S/N.

[0051]

The signal and the noise are evaluated by reading in accordance with the method mentioned above. As a result, it is possible to obtain a high S/N satisfying a relation dynamic range (S/N) in each of bits = 75 to 85 dB.

Embodiment 4

25 [0052]

A description will be given of a fourth embodiment in accordance with the present invention

with reference to Fig. 7. Fig. 7 is a view of a cross sectional structure of a CCD image sensor using the present invention. A carrier from the photodiode passes through a potential well and is transferred at  
5 a clock of  $\phi 1$  and  $\phi 2$ .

[0053]

In a final stage, a diffusion floating region FD 907 is formed in a lower portion of a side surface of a gate region 903 of the transfer MOS transistor, and the diffusion floating region FD 907 is connected  
10 to a gate of an amplifying MOS transistor of an output circuit, and outputs as a source follower amplifier circuit. The  $1/f$  noise is reduced by using the buried channel type MOS transistor as a  
15 transistor 910 of the source follower.

[0054]

Further, a source of a reset MOS transistor 908 for resetting the diffusion floating region FD 907 is connected to the diffusion floating region FD 907, and a reset power source 909 is connected to a drain  
20 thereof. The other MOS transistors than the source follower transistor are constituted by the surface channel type MOS transistor in this case. The preparing method of the surface channel type MOS  
25 transistor of the same type of the buried channel type MOS transistor and the like are the same as the embodiment mentioned above, the present invention is

also applied to the CCD structure, and it is known that a great effect that the noise is reduced can be obtained.

Embodiment 5

5 [0055]

Fig. 8 shows an example of a circuit block in the case that the solid state image pickup device in accordance with the present invention is applied to a camera. A shutter 1001 is provided in front of an  
10 image pickup lens 1002, and controls an exposure. A light intensity is controlled by a diaphragm 1003 as occasion demands, and an image is formed in a solid state image pickup device 1004. A signal output from the solid state image pickup device 1004 is processed  
15 by a signal processing circuit 1005, and is converted into a digital signal from an analogue signal by an A/D converter 1006. The output digital signal is arithmetically operated further by a signal processor 1007. The processed digital signal is stored in a  
20 memory 1010, and is sent to an external device through an external I/F unit 1013. The solid state image pickup device 1004, the image pickup signal processing circuit 1005, the A/D converter 1006 and the signal processor 1007 are controlled by a timing  
25 generator 1008, and an entire of the system is controlled by a unit controlling a whole and arithmetic operation 1009. In order to record the

image in a recording medium 1012, the output digital signal is recorded through an I/F unit controlling recording medium 1011 controlled by the entire control portion and arithmetically operating portion.

5

[Brief Description of the Drawings]

[0056]

[Figure 1] A view showing an embodiment in accordance with the present invention.

10 [Figure 2] Cross sectional views showing a first embodiment in accordance with the present invention.

[Figure 3] A view showing an impurity profile of the first embodiment in accordance with the  
15 present invention.

[Figure 4] Cross sectional views showing a second embodiment in accordance with the present invention.

[Figure 5] A view of an equivalent circuit of a  
20 pixel in a solid state image pickup device.

[Figure 6] A view of an equivalent circuit including a reading circuit of an area sensor using the present invention.

[Figure 7] A cross sectional view showing a  
25 fifth embodiment in accordance with the present invention.

[Figure 8] A block diagram of a structure of a

camera system using the solid state image pickup device in accordance with the present invention.

[Description of Reference Numerals or Symbols]

[0057]

- 5 101, 201, 401, 901: substrate
- 102, 202, 402, 902: well
- 103, 203, 209, 403, 903: control electrode
- 104, 204, 404: photodiode part
- 107, 907: diffusion floating region
- 10 108, 908: resetting MOS transistor
- 109, 501, 801, 909: power source
- 110, 910: source follower transistor
- 111: transistor for line selection switch
- 112, 812: current source
- 15 113: output terminal
- 114, 205, 405, 914: first channel doped layer
- 115, 206, 406: second channel doped layer
- 207, 407: surface layer
- 208, 408: photo-resist layer
- 20 410: deep well
- 502, 802: reset switch line
- 503, 803: selection switch line
- 504, 804: signal output line
- 505: photodiode
- 25 506, 813: transfer switch line
- 805: signal storage unit
- 808: transfer switch to a common signal line 1

808': transfer switch to a common signal line 2

809: common signal line 1

809': common signal line 2

810: output amplifier

. 5 811: output 1

811': output 2

906: charge transfer unit well

[Name of the Document]    Abstract

[Abstract]

[Subject] To provide a semiconductor device which is reduced in noise by forming a highly controllable transistor by a simple process and a method of manufacturing the same.

[Solving Means] A photoelectric conversion device is constructed such that a p-type well 102 is formed on an n-type substrate 101, an n-type layer 104 of a photodiode is formed on the well 102, a p-type layer 105 of the photodiode is formed on the layer 104 so as to make the density of impurity on the surface dense and a gate region 103 of a transfer MOS transistor is formed thereon via an insulating layer. A diffusion floating region FD 107 is formed under a side face of the gate region 103 and is connected to a gate of an amplification MOS transistor of an output circuit, a drain of a line selection switch MOS transistor 111 is connected to a source of the amplification MOS transistor and a current source 112 is connected to a source of the MOS transistor 111 to constitute a source follower amplification circuit. A buried channel type MOS transistor is used as a transistor 110 of the source follower amplification circuit to reduce 1/f noise.

[Elected Drawing]    Figure 1